REMARKS/ARGUMENTS

Applicants have received the Office action dated April 10, 2006, in which the Examiner: 1) objected to claim 1; 2) rejected claims 1-3, 5-15 and 17-24 under 35 U.S.C. § 103(a) as being unpatentable over Roscoe et al. (U.S. Pat. No. 6,498,731, hereinafter "Roscoe") in view of Wallace et al. (U.S. Pat. No. 6,628,537, hereinafter "Wallace") and further in view of Baker et al. (U.S. Pat. No. 6,819,567, hereinafter "Baker"). With this Response, Applicants have amended claims 1, 14, and 22.

Claim 1 has been amended to include a first circuit board and a second circuit board, and thereby overcome the objection to claim 1.

Applicants have amended claims 1, 14, and 22 to more particularly claim the arrangement of components when the memory package is in a closed position. Claim 1 has been amended to include at least one memory module socket projecting from a surface of the first circuit board, at least one memory module socket projecting from a surface of the second circuit board, and a memory module socket mounted to the first circuit board is in an opposed relationship with an adjacent controller chip mounted to the second circuit board and a memory module socket mounted to the second circuit board is in an opposed relationship with an adjacent controller chip mounted to the first circuit board.

The Examiner relies on Roscoe to teach an electronic assembly having a memory module socket, or memory module, mounted to a circuit board supported by a cover portion. The Examiner concedes that Roscoe does not teach a controller chip mounted to a circuit board nor a second electronic assembly mounted to a second cover portion. The Examiner relies on Wallace to teach a controller chip disposed on the circuit board, and further relies on Baker to teach an electronic assembly mounted to a second cover portion. The Examiner also concedes that Roscoe does not teach the memory module socket, or memory module, on a first circuit board is placed adjacent a controller chip mounted on a second board, and a memory module socket, or memory module, on a second board is placed adjacent a controller chip mounted on a first circuit board. As to

this element of claim 1, the Examiner contends that one having skill in the art would have been motivated to place the controller chip of Wallace in a slot adjacent to a memory module socket of Roscoe. However, there are no teachings in either Roscoe, Wallace or Baker disclosing at least one memory module socket projecting from a surface of the first circuit board, at least one memory module socket projecting from a surface of the second circuit board, and a memory module socket mounted to the first circuit board is in an opposed relationship with an adjacent controller chip mounted to the second circuit board and a memory module socket mounted to the second circuit board is in an opposed relationship with an adjacent controller chip mounted to the first circuit board. The Examiner has not cited any other teachings or motivation for making the claimed arrangement.

Roscoe does not teach a memory module socket projecting from a surface of a circuit board. Socket 208 cited by the Examiner is coplanar with the circuit board 210. Nor does Roscoe teach a memory module socket mounted to a first circuit board (which is part of a first electronics sub-assembly supported by a first cover portion—see claim 1) being in an opposed relationship with an adjacent controller chip mounted to a second circuit board (which is part of a second electronics sub-assembly supported by a second cover portion—see claim 1). Roscoe teaches a plurality of circuit boards coplanar with a socket and a memory module supported by a single cover portion. Placing the controller chip of Wallace adjacent a memory module socket of Roscoe means the controller chip is supported by the same cover portion. Thus, Roscoe cannot teach a memory module socket supported by a first cover portion being in an opposed relationship with an adjacent controller chip supported by a second cover portion.

The particular arrangement of components of claim 1 cannot be gleaned from the prior art references cited by the Examiner for, absent the Applicants' specification, there simply is no motivation to arrange components as recited in claim 1. *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984) ("The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself

sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device."); MPEP 2144.04(VI)(C). Nor do the cited disclosures taken as a whole suggest the desirability to one of ordinary skill in the art the particular arrangement of components as recited in claim 1.

Therefore, claim 1 is not rendered obvious by the cited combination. Claims 2-13 depend from claim 1 and are also not rendered obvious by the cited combination. Therefore, claims 1-13 are allowable over the cited art.

Claim 14 has been amended to include the memory module projecting from the circuit board beyond the memory controller, wherein the memory module mounted to the first circuit board is opposed to the memory controller mounted to the second circuit board, the memory module mounted to the second circuit board is opposed to the memory controller mounted to the first circuit board, and the memory modules are located side-by-side. Claim 22 has been amended to include the memory module projecting from the sub-assembly beyond the memory controller chip, wherein the memory module mounted to the first electronics sub-assembly is opposed to the memory controller chip mounted to the second electronics sub-assembly, the memory module mounted to the second electronics sub-assembly is opposed to the memory controller chip mounted to the first electronics sub-assembly, and the memory modules are located side-by-side.

Roscoe nor any other cited references teaches these claimed arrangements. Claim 14 includes a first circuit board coupled to at least one memory module projecting from the first circuit board beyond the memory controller, wherein the first circuit board is supported by a first cover portion, and a second circuit board coupled to at least one memory module projecting from the second circuit board beyond the memory controller, wherein the second circuit board is supported by a second cover portion. Further, claim 14 includes that the memory module mounted to the first circuit board is opposed to the memory controller mounted to the second circuit board, and the memory modules are

located side-by-side. Roscoe, as previously shown, does not teach a memory module projecting beyond a memory controller. Also, Roscoe teaches memory modules and controller chips extending from only one cover portion. Therefore, Roscoe cannot teach a memory module supported by a first cover portion opposing a memory controller supported by a second cover portion, or a memory module supported by a first cover portion side-by-side with a memory module supported by a second cover portion. Nor do any of the other cited references teach or motivate one skilled in the art to make the claimed arrangement.

Amended claim 22 is not taught by the cited art. Particularly, Roscoe does not teach a memory module projecting beyond a memory controller chip. Roscoe also does not teach the claimed memory module opposing a memory controller chip or the claimed memory modules located side-by-side.

Therefore, claims 14 and 22 are not rendered obvious by the cited combination. The remainder of the pending claims depend from one of claims 14 or 22 and are also not rendered obvious by the cited combination. Therefore, claims 1-3, 5-15, and 17-24 are allowable over the cited art.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are

hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

Matthew R. Moscicki
PTO Reg. No. 57,524
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400